REMARKS

Claims 1 through 94 are currently pending in the application.

Claims 3, 6 through 16, 18, 19, 21, 24, 27 through 34, 36, 37, 39, 41 through 44, 47, 49 through 62, 67-79 and 81-94 have been withdrawn from consideration as being directed to a non-elected invention.

Claims 1-2, 4, 5, 17, 20, 22, 23, 25-, 26, 35, 38, 40, 45-, 6, 48, 63 through 66, and 80 were rejected.

Drawings

Applicants submit herewith, under cover of a separate Transmittal of Formal Drawings, FIGS. 12B and 12C which were inadvertently not included with the Formal Drawings which were previously filed on August 24, 2001. Applicants respectfully request approval of the drawings.

35 U.S.C. § 103(a) Rejection

Claims 1, 2, 4, 5, 17, 20, 22 through 23, 25, 26, 35, 38, 40, 45, 46, 48, 63 through 66, and 80 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Khandros et al. (U.S. Patent 5,998,864) in view of Burns (U.S. Patent 5,585,668).

Applicants submit that M.P.E.P. § 706.02(j) clearly sets forth the standard for a § 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic requirements must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Khandros et al teaches or suggests resilient electrical contact elements for use in forming pressure connections between electronic components. In particular, Khandros et al. teaches or suggests microminiature spring contacts for probing microelectronic components. (Col. 1, lines 26-32). The semiconductor memory chips are stacked atop one another so that an edge of each semiconductor device is exposed. The free-standing elongated interconnect elements are long enough to make contact with terminals on the substrate to which the semiconductor devices are mounted. (Col. 6, lines 22-34). Each semiconductor device is individually connected to the substrate. (Col. 6, lines 34-39). Semiconductor devices at or near the top of the stack of semiconductor devices have interconnection elements longer than devices lower in the stack. (Co. 7, lines 4-10).

Burns teaches or suggests an integrated circuit package with overlapped die on a common lead frame. (Title). An upper integrated circuit die 12 is laminated to a common lead frame 16. A second integrated circuit die 14 is laminated to an opposite side of common lead frame 16. (FIG. 1, Col. 2, lines 32-37). Upper integrated circuit die 12 and lower integrated circuit die 14 are both mounted with their active surfaces facing a common lead frame 16. (Col. 2, lines 38-41). The integrated circuit die are slightly offset from each other so the wire bond pads 18 on each die are exposed and accessible for wire bonding. (Col. 2, lines 42-43). The double die and common lead frame assembly is encased with an injected plastic transfer molding material 32. (Col. 3, lines 37-39). The resulting package is then lapped to the desired thickness. (Col. 3, lines 44-46).

Applicants respectfully submit that any combination of Khandros et al. and Burns fail to teach or suggest the limitations of the claimed inventions set forth in independent claims 1, 22, 45, and 63 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention of a stacked multiple die or multiple semiconductor device where the claimed invention calls for "the backside of a first semiconductor die being attached to the surface of the substrate adjacent the at least one conductive bond area of said surface of the substrate and the backside of a second semiconductor die is attached to the active surface of the first semiconductor die in an offset position having the field of conductive bond pads of the first semiconductor die exposed" and calls for "conductors connecting bond pads of the second semiconductor die to one of the conductive bond areas of the substrate and conductive bond pads

of the first semiconductor die". Khandros does not teach or suggest an offset structure. Connections in Khandros are made directly to the substrate, not to the stacked semiconductor dies. In addition, the electrical connections of Khandros are spring contacts for probing. Probing uses resilient, temporary contacts for testing purposes. Thus, the semiconductors in Khandros are not electrically connected to one another, nor are permanent connections formed. Burns teaches or suggests mounting the semiconductor dies on opposite sides of a substrate. While the devices are offset, the devices are not stacked on top of one another as in Applicants' claimed inventions. Furthermore, Burns teaches or suggests that both semiconductors are attached to a lead frame which routes the electrical signals from the device. The lead frame connects the semiconductor devices to the substrate, not to one another. Having failed to teach or suggest each and every limitation of the claims, the cited prior art cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Applicants submit that the references themselves teach away from any proposed combination thereof whatsoever and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because Khandros teaches or suggests temporary connections for probing the semiconductor devices and connects directly to the substrate using longer leads, while Burns teaches or suggests connecting the semiconductor devices to a lead frame and then attaching the lead frame to the substrate. It would not be obvious to one of ordinary skill in the are to combine Khandros and Burns because it would not be possible to connect the stacked semiconductor devices of Khandros to the lead frame of Burns using elongated leads and temporary testing contacts.

Accordingly, any combination of Khandros and Burns cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

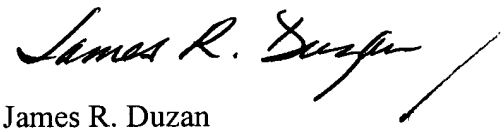
Claims 2, 4, 5, 17, 23, 25, 26, 35, 38, 40, 46, 64, 66, and 80 are each allowable as depending , either directly or indirectly from allowable claims 1, 22, 45, and 63.

ENTRY OF AMENDMENT

Applicants submit that claims 1, 2, 4, 5, 17, 20, 22-23, 25, 26, 35, 38, 40, 45, 46, 48, 63 through 66, and 80 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1, 2, 4, 5, 17, 20, 22-23, 25, 26, 35, 38, 40, 45, 46, 48, 63 through 66, and 80 and the case passed for issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A stacked multiple-semiconductor die device, comprising:

a substrate having a surface;

at least one conductive bond area on the surface of the substrate;

a plurality of semiconductor dice having similar dimensions, each semiconductor die having an active surface including at least four edges, and a backside;

a field of conductive bond pads disposed on the active surface of each semiconductor die, the field of conductive pads positioned along less than three edges of the active surface of a semiconductor die, the backside of a first semiconductor die being attached to the surface of the substrate adjacent the at least one conductive bond area[s] of said surface of the substrate and the backside of a second semiconductor die is attached to the active surface of the first semiconductor die in an offset position having the field of conductive bond pads of the first semiconductor die exposed;

conductors connecting bond pads of the first semiconductor die to conductive bond areas of the substrate; and

conductors connecting bond pads of the second semiconductor die to one of the conductive bond areas of the substrate and conductive bond pads of the first semiconductor die.

35. (Amended) The high density stacked multiple-die device of claim [34] 26, wherein each semiconductor die has a field of bond pads along two adjacent edges thereof, and each of the second and subsequent semiconductor die is offset from its underlying semiconductor die in two directions exposing the bond pads thereof for conductive bonding and;

each semiconductor die is offset in the same two directions relative to its underlying semiconductor die.